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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/789,637 | 02/27/2004 | Brian S. Schieck | NVID-P001125 | 7655 |

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| EXAMINER | |
|---|---|
| DUONG, KHANH B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/789,637 | SCHIECK ET AL. | |
| | Examiner | Art Unit | |
| | Khanh B. Duong | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *8-12 and 19-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/16/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election **without** traverse of Group I, Claims 1-7 and 13-18 in the reply filed on November 18, 2005 is acknowledged.

Claims 8-12 and 19-35 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim.

Accordingly, claims 1-7 and 13-18 are active.

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on August 16, 2005 is being considered by the examiner.

### *Specification*

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: A FLIP CHIP SEMICONDUCTOR DIE INTERNAL SIGNAL ACCESS SYSTEM.

### *Claim Objections*

Claim 5 is objected to because of the following informalities: line 1, after "said FIB pad is", "a" is informal and should be deleted.

Appropriate correction is required.

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1 and 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al. (U.S. Patent No. 6,686,615), submitted by Applicant.**

Re claim 1, Cheng et al. ("Cheng") discloses in FIGs. 2-4 a semiconductor die 10 comprising: a test signal redistribution layer (14, 21 and 30) comprising conductive traces 21; a test probe point 12 for accessing signals in said semiconductor die 10 and for electrical coupling to said test signal redistribution layer; and a conductive bump 40 for transmitting said signals off of said semiconductor die 10, said conductive bump 40 located on a first surface of said semiconductor die 10 and electrically coupled to said test signal redistribution layer.

Re claims 3-5, the claims recite the following product-by-process limitations: "accessible by drilling" (claim 3); "a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill" (claim 4); and "conductive material backfill" (claim 5). However, these limitations have not been given patentable weight because product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. "[E]ven though product-by-process claims are limited by and defined by the process,

determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). Thus, Cheng discloses in FIG. 3 the test probe point 12 comprises a bonding pad 12 which is coupled to said test signal redistribution layer (14, 21 and 30).

**Claims 13, 14 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (U.S. Patent No. 5,258,648), submitted by Applicant.**

Re claim 13, Lin discloses a semiconductor device in FIGs. 1-5 comprising: a package substrate 22 for communicating test signals on an external access point 28; and a semiconductor die 12 having test probe points 16 accessible by said external access point 28, wherein said semiconductor die 12 is electrically coupled to said package substrate 22.

Re claim 14, Lin expressly discloses in FIG. 5 said package substrate 22 comprises: a first surface with ball grid array 32; a second surface with conductive contacts 26 for electrically coupling with conductive bumps 16 of said semiconductor die 12; and a trace for electrically coupling one of said conductive contacts 26 to said external access point 28 [see also col. 7, lines 10-27].

Re claim 18, Lin discloses said external access point 28 is accessible by automatic test equipment [see col. 7, lines 25-27].

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Lin.**

Re claim 2, Cheng expressly discloses in FIG. 3 that said semiconductor die is a flip chip die configured for connection to an inherent package substrate. However, Cheng **fails** to

specifically mention the conductive bump being electrically coupled to a test signal access component of a package substrate.

Lin teaches in FIG. 5 to electrically couple the conductive bumps 16 of a semiconductor die 12 to a test signal access component 28 of a package substrate 22 [see col. 7, lines 10-27].

Since Cheng and Lin are from the same field of endeavor, the purpose disclosed by Lin would have been recognized in the pertinent prior art of Cheng.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Cheng as taught by Lin, since Lin states at column 7, lines 27-31 that such modification would allow the composite flip chip semiconductor device to be tested and burned-in in a known test socket which is capable of handling edge contacts.

**Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Cheng.**

Re claims 15 and 17, Lin **fails** to disclose said semiconductor die comprises: a test signal redistribution layer comprising conductive traces; a test probe point for accessing signals in said semiconductor die and for electrical coupling to said test signal redistribution layer; a test access via for electrically coupling said test probe point to said test signal redistribution layer; and a conductive bump for conveying a test signal off of said semiconductor die to said package substrate, said conductive bump located on a first surface of said semiconductor die and electrically coupled to said test signal redistribution layer. Lin further **fails** to disclose routing of said test signal redistribution layer conductive traces is such that trace widths and spacing is a minimum without causing signal interference.

Cheng shows in FIGs. 2 and 3 a semiconductor die 10 comprises: a test signal redistribution layer (14, 21 and 30) comprising conductive traces 21; a test probe point 12 for accessing signals in said semiconductor die 10 and for electrical coupling to said test signal redistribution layer; a test access via (on 12) for electrically coupling said test probe point 12 to said test signal redistribution layer; and a conductive bump 40 for conveying a test signal off of said semiconductor die 10 inherently to a package substrate, said conductive bump 40 located on a first surface of said semiconductor die 10 and electrically coupled to said test signal redistribution layer [see col. 2, line 41 to col. 3, line 40]. Cheng further appears to expressly disclose in FIG. 2 said test signal redistribution layer conductive traces 21 are routed such that trace widths and spacing is a minimum without causing signal interference.

Since Lin and Cheng are from the same field of endeavor, the purpose disclosed by Cheng would have been recognized in the pertinent prior art of Lin.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the device disclosed by Lin as suggested by Cheng , since Cheng states at column 1, lines 55 to 58 that such modification would form redistribution traces having equal lengths to acquire simple circuit design to reduce signal skew.

Re claim 16, the claim recites the following product-by-process limitations: "a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill". However, these limitations have not been given patentable weight because product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does

not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references disclose relevant teachings regarding flip chip die having test signal redistribution layer: Hembree '555, Farnworth '087 and Farnworth '642.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

Zandra V. Smith
Supervisory Patent Examiner
5/1/2006